IN THE SPECIFICATION

Please amend the Title on page 1 as follows:

MULTI-USER RECEIVING METHOD AND RECEIVER

Please replace the paragraph at page 21, line 27 – page 22, line 5, with the following rewritten paragraph:

The signal extractors may switch output user signals in addition to adaptively estimating coefficients of the signal extractors. FIG. 5 shoes a fifth configuration example of the receiver of the first embodiment. The receiver adaptively estimates coefficients of the signal extractors on the basis of received signals and signal series from the series estimator, and user signals output from the signal extractors are switched. Compared with the receiver shown in FIG. 1, K stages of adaptive controllers 7-1 – 7-K, a state estimator 9 and switch circuits ~~10-1-10-k-1~~ 10-1 – 10-K -1 are provided to the receiver shown in FIG. 5. The operations of the adaptive controllers 7-1 – 7-K, the state estimator 9 and switch circuits 10-1 – 10-K-1 are the same as those of FIG. 2 and FIG. 4.

Please replace the paragraph at page 23, lines 18 – 30, with the following rewritten paragraph:

More concretely, like the series estimator in the first embodiment, when the added value calculated by the adder 24 is not the maximum value, the series estimator 25 estimates each signal series for each of first to Kth user signals and outputs the signal series to each likelihood estimator. The likelihood estimator calculates log likelihood function on the basis of this signal series and user signals extracted by the same stage signal extractor. Then, the adder [[4]] 24 adds the log likelihood functions. When the added value is still not maximum, the series estimator 25 estimates and outputs signal series to the likelihood estimators again.

Please replace the paragraph at page 23, lines 31 – 36, with the following rewritten paragraph:

By repeating this operation, when the added value calculated by the adder [[4]] 24 becomes maximum, the series estimator 25 determine each signal series estimated just before as first – Kth user sending signal series, and outputs the signals to the output terminals 26-1 – 26-K.

Please replace the paragraph at page 29, lines 3 – 14, with the following rewritten paragraph:

When assuming that a received signal of the feeding element of the array antenna is $u_i(k)$ (i is a number corresponding to a feeding element), and an output signal of the signal extractor is r_k, $r_i(k) = j = 1\ N_{et}\ v^*_{i,j}\ (k)\ u_j\ (k)\ (8)$ is satisfied, wherein ~~$v_{k,j}$ (i)~~ $v_{i,j}$ (k) represents the weight coefficient for multipliers in the signal extractor, N.sub.el represents the number of antenna elements. At this time, when $d_i(k)$ is tentative decision data from the tentative decision data input terminal 66-K+1, the difference between the replica and the output signal of the signal extractor can be represented as follows.

Please replace the paragraph at page 30, line 32 – page 31, line 8, with the following rewritten paragraph:

FIG. 17 shows a configuration example of the switch circuit. The switch circuit shown in the figure outputs i-1 signals for i input signals. The switch circuit includes input terminals 81-1 – 81-i, a body 82 of the switch circuit, nodes 83-1 – 83-i, 84-1 – 84-i-1, a switch control terminal 85, and output terminals 86-1 – 86-i-1. In the example shown in FIG. 17, a signal from the input terminal 81-2 is disconnected and other signals are output.

Please replace the paragraph at page 31, line 25 – page 32, line 13, with the following rewritten paragraph:

FIG. 18 shows a first configuration example of the series estimator. The series estimator shown in the figure is an example for two users each of which users uses ~~QPSK~~ Quadrature Phase Shift Keying (QPSK), and this example is for the case that there is no memory in the communication channel. The series estimator includes an input terminal 91, a lowest value detector 92, a reset terminal 93, binary counters 94-1, 94-2, memory circuits 95-1, 95-2, tentative decision data output terminals 97-1, 97-2 and demodulated signal output terminals 99-1, 99-2. The lowest value detector 92 and the binary counters 94-1, 94-2 are reset in synchronization with a reset signal from the reset terminal 93 in a symbol period. Therefore, the lowest value detector 92 detects a minimum value in a symbol. Since f_c in FIG. 18 represents a symbol frequency, the two binary counters 94-1 and 94-2 generates every pattern of QPSK. Therefore, the lowest value detector 92 estimates the lowest combination in every signal pattern to be transmitted by the two users, extracts the combination from the memory circuits 95-1 and 95-2, and outputs the combination from the demodulated signal output terminals 99-1 and 99-2.

Please replace the paragraph at page 32, lines 27 – 34, with the following rewritten paragraph:

FIG. 20 shows a configuration example of the tapped delay line used for the signal extractor shown in FIG. 19. The tapped delay line shown in FIG. 20 includes a signal input terminal 111, delay elements ~~112-1 – 112-4~~ 112-1 – 112-3, multipliers 113-1 – 113-4, weight coefficient input terminals 114-1 – 114-4 for the multipliers, an adder 115 and a signal output terminal 116.

Please replace the paragraph at page 33, lines 11 – 22, with the following rewritten paragraph:

FIG. 22 shows a second configuration example of the adaptive controller, which is an example when using the signal extractor shown in FIG. 21. The adaptive controller shown in FIG. 22 includes a coefficient output terminal 131 to the signal extractor, signal input terminals 132 from the signal extractor, an adder 134, a subtracter 135, feedback filters ~~136-1 – 136-N~~ 136-1 – 136-K each formed by the tapped delay line shown in FIG. 20, tentative decision data input terminals 137-1 – 137-K+1 from the series estimator and an adaptive algorithm part 138.

Please replace the paragraph at page 34, lines 19 – 33, with the following rewritten paragraph:

FIG. 24 shows a fifth configuration example of the signal extractor which is for CDMA communication. The signal extractor shown in FIG. 24 includes a signal input terminal 201, a matched filter 202 for despreading, an orthogonal filter 203, a signal output terminal 204 for outputting a signal after despread, a coefficient input terminal 205 to the orthogonal filter and a signal output terminal 206. According to this signal extractor, after despreading is performed by the matched filter 202 which has code sequence of a signal desired to be extracted as tap coefficient, undesired interference component included in the output is filtered by the orthogonal filter 203 so that only desired signal group can be obtained.

Please replace the paragraph at page 34, line 34 – page 35, line 5, with the following rewritten paragraph:

FIG. 25 is a sixth configuration example of the signal extractor in which the matched filter 202 and the orthogonal filter 203 are integrated to an orthogonal filter 213. The signal extractor shown in FIG. 25 includes a signal input terminal 211, an orthogonal filter 213, a received signal output terminal 214 to the adaptive controller, a coefficient input terminal 215 to the orthogonal filter and a signal output terminal 216 ~~206~~.

Please replace the paragraph at page 35, lines 6 – 21, with the following rewritten paragraph:

FIG. 26 shows a third configuration example of the adaptive controller for using the signal extractor shown in FIG. 24 and FIG. 25. The adaptive controller in FIG. 26 includes a coefficient output terminal 221 to the signal extractor, a signal input terminal 222 from the signal extractor, an adder 224, a subtracter 225, multipliers 226-1 – 226-K, tentative decision data input terminals 227-1 – 227-K+1 from the series estimator, and an adaptive algorithm part 228. If ~~$S_k(i)$~~ $\underline{w^*_{i,j}(k)\, d_j(k)}$ in the equation (9) is regarded as a signal from the multiplier 226-1, and $U_i(k)$ in the equation (10) is regarded as data vector to shift register of the tapped delay line of the orthogonal filter 213, the adaptive controller can perform coefficient estimation by using the equation (10).

Please replace the paragraph at page 36, lines 27 – 36, with the following rewritten paragraph:

FIG. 31 shows a characteristics example of the receiver of FIG. 11 in which the signal extractor of FIG. 21, the adaptive controller of FIG. 22, and the series estimator of FIG. 23 are applied, and characteristics example when using adaptive array, in which four element array antenna is used. Also in FIG. 31, two cases of flat Rayleigh fading channel and two

path ~~pass~~ Rayleigh fading are shown for the communication channel. In addition, QPSK is used for the modulation method.